Applicant appreciates the courtesies shown to Applicant's representative by Examiner Soward in the August 7, 2002 interview. Applicant's separate record of the substance of the interview is incorporated into the following remarks.

I. Objection to the Specification

The specification was objected to by the Patent Office for allegedly not reciting that "This application is a 371 of PCT/JP00/06624 filed 09/29/00" in the first page of the specification. The objection is respectfully traversed.

By this Amendment, the specification is amended to recite that "This application, under 35 U.S.C. §371, is a U.S. National Stage application of PCT/JP00/06624 filed September 29, 2000."

In view of the foregoing amendment to the specification, Applicant respectfully requests reconsideration and withdrawal of the objection.

II. Rejection Under 35 U.S.C. §112, Second Paragraph

Claim 16 was rejected by the Patent Office under 35 U.S.C. §112, second paragraph for allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regard as the invention. Applicant respectfully traverses the rejection.

In particular, the Patent Office alleges that the wording of claim 16 is not clear.

By this Amendment, claim 16 is amended to recite that a circuit board is mounted on the semiconductor device.

Applicant submits that claim 16 clearly points out and distinctly claims the subject matter which Applicant regards as the invention, and thus fully complies with the requirements of 35 U.S.C. §112, second paragraph.

In view of the foregoing amendment to claim 16, reconsideration and withdrawal of the rejection are respectfully requested.

III. Rejection Under 35 U.S.C. §103(a)

Claims 1-20 were rejected by the Patent Office under 35 U.S.C. §103(a) as allegedly being obvious over U.S. Patent No. 5,117,282 to Salatino (hereinafter "Salatino"). The rejection is respectfully traversed.

Salatino fails to teach or suggest the present invention. Instead, Salatino teaches "stacking of a plurality of integrated circuit devices by employing a web of flexible interconnect material that is readily folded into a 'layered' arrangement of parallel web fingers onto which a plurality of integrated circuit devices may be mounted." (See column 1, lines 31-35).

In other words, Salatino teaches a second portion that is to be superposed on a first portion but the second portion has a shape such that it protrudes from the first portion when the second portion is superposed on the first portion.

Salatino fails to teach or suggest "an interconnect substrate over which an interconnect pattern is formed, comprising: a first portion; and a second portion to be superposed on the first portion, wherein the first portion has an end part as a positioning reference; and wherein the second portion has a shape so as to be superposed on and inside the first portion except the end part" as recited in claim 1 of the present application. (Emphasis added). In particular, Salatino fails to teach or suggest that the second portion has a shape so as to be superposed on and inside the first portion.

Salatino describes that each web finger is spaced such that "when folded on top of one another as shown in Figs. 3 and 4, the web fingers are mutually aligned in a stack." (See column 2, lines 58-59) (Emphasis added).

Applicant urges the Patent Office to see Fig. 4 of Salatino, wherein web fingers 21 and 22 are fully aligned and superposed over each other. There is not a portion of either web finger 21 or 22 that is superposed on and inside the opposing web finger.

The present invention, however, claims that "the second portion has a shape so as to be superposed on and inside the first portion except the end part." (See claim 1) (Emphasis added).

For the foregoing reasons, Applicant submits that Salatino fails to teach or suggest the present invention. Reconsideration and withdrawal of the rejection are respectfully requested.

IV. Conclusion

In view of the foregoing amendments and remarks, Applicant submits that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-20 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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Registration No. 27,075

David M. Lafkas
Registration No. 50,424

JAO:DML/rxg

Attachment:
Appendix

Date: August 8, 2002

OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
Charge any fee due to our Deposit Account No. 15-0461

APPENDIX

Changes to Specification:

Page 1, between lines 4 and 5, a new paragraph is added.

Changes to Claims:

The following is a marked-up version of the amended claims:

1. (Amended) An interconnect substrate over which an interconnect pattern is formed, comprising:

a first portion; and

a second portion to be superposed on the first portion,

wherein the first portion has an end part as a positioning reference; and

wherein the second portion has a shape so as to be superposed on and inside the first portion except the end part.

13. (Amended) A semiconductor device comprising:

at least one semiconductor chip; and

a substrate which has a first portion and a second portion to be superposed on the first portion, and on which the semiconductor chip is mounted,

wherein the first portion includes an end part as a positioning reference; and

wherein the second portion has a shape ~~which avoids~~ so as to be superposed inside the first portion and avoid being superposed over the end part of the first portion.

15. (Amended) The semiconductor device as defined in claim 13,

wherein the interconnect substrate as defined in ~~any one of claims~~ claim 1 ~~to 10~~ is used as the substrate.

16. (Twice Amended) A circuit board ~~over~~ on which is mounted the semiconductor device as defined in claim 13.